REMARKS

Applicant respectfully requests reconsideration of this application, as amended herein, and reconsideration of the Office Action dated September 13, 2002.

Upon entry of this Amendment, claims 2, 9-11, 17, 19, 21, and 22 will remain pending in this application.

Applicant acknowledges, with appreciation, the Examiner's indication that claims 9-11, 17, and 21 contain patentable subject matter. In view of this Amendment and the following remarks, Applicant respectfully submits that all of the remaining claims in this application stand in condition for immediate allowance. The various issues raised in the September 13, 2002, Final Office Action are addressed in detail below.

I. The Drawing Objection

The Examiner objected to Fig. 6, alleging that the drain of transistor 122 should be shown as an output rather than ground. Applicant respectfully submits that the down arrow symbol used in Fig. 6 correctly illustrates, in a conventional manner, that the drain of transistor 122 is pulled to a lower voltage than the transisotor's gate. Accordingly, Applicant respectfully requests that the Office withdraw this objection.

II. Double Patenting

The Examiner advised Applicant that if claim 1 were found to be allowable, claim 22 would be objected to under 37 C.F.R. § 1.75 as being a substantially duplicate claim. This objection is not

understood because claim 1 was canceled from this application in a Preliminary Amendment dated January 23, 2002. Accordingly, this objection, as stated, cannot stand.

Applicant notes, however, that the content of claim 22 is similar to that contained in claim 2. These claims, however, are not identical in scope. Specifically, claim 22 recites that the compensation circuit is "configured to increase the mirror current against a decrease of absolute value of a drain voltage of the second MOS transistor." Claim 2, on the other hand, recites that the compensation circuit is "configured to decrease the mirror current against an increase of absolute value of a drain voltage of the second MOS transistor." Because these claims are not of identical scope, Applicant respectfully submits that claims 2 and 22 can properly co-exist in this present application. Withdrawal of this objection is respectfully requested.

III. Rejection Based On 35 U.S.C. § 112, First Paragraph

Claims 2, 9-11, 17, 19, 21, and 2 [sic., presumably 22] are rejected under 35 U.S.C. § 112, first paragraph, as allegedly based on a non-enabling disclosure. Applicant respectfully traverses this rejection and requests its reconsideration.

As an initial matter, Applicant notes that the Examiner has included claims 2, 9-11, 17, and [presumably] 22 in this rejection. However, no portion of this rejection describes or even alleges any deficiencies specific to claim 2, 9-11, 17, or 22. Rather, the discussion of this rejection mentions only independent claims 19 and 21. Because this rejection does not identify any deficiencies relating to claims 2, 9-11, 17 and 22, the rejection of these claims cannot stand. Withdrawal of the rejection of claims 2, 9-11, 17, and 22 on this basis is respectfully requested.

As to claims 19 and 21, the Examiner alleges that these claims are deficient for failing to recite input transistors and/or a current source, elements the Examiner alleges to be critical or essential to the practice of the invention. Applicant respectfully submits that the specification fully describes and enables the circuits as defined in claims 19 and 21 such that no further amendment in this regard is necessary.

At least some aspects of the present invention relate to circuits that include compensation circuits. Examples of such circuits according to these aspects of the invention include current mirror circuits and current source circuits. Accordingly, claims in this patent application are directed to both current mirror circuits and current source circuits.

In stating this rejection, the Examiner refers to Figs. 7 and 14. Figs. 4, 7, and 14 illustrate examples of current mirror circuits according to this invention that include compensation circuits. Specifically, Fig. 4 illustrates an example of a current mirror circuit having transistors 111 and 112 and a compensation circuit 114. Fig. 7 illustrates a current mirror circuit having transistors 111 and 112 and a compensation circuit including subtracters 141_1 to $141_{(n-1)}$ and transistors 113_1 to $113_{(n-1)}$. Fig. 14 illustrates an example of a current mirror circuit having transistors 121, 122, 125, and 126 and compensation circuits including subtracters 129 and 130 and transistors 127 and 128. Such current mirror circuits, as illustrated in Figs. 4, 7, and 14 and described in the present specification, may include current sources, like current source 115 shown in these figures.

In contrast to the current mirror circuits of Figs. 4, 7, and 14, independent claims 19 and 21 relate to current source circuits. As described in Paragraphs 67-69 in the present specification, while current source circuits may be connected with a current source during use, the current source circuit

itself, as it is described and illustrated in this application, need not include a current source. Figs. 16 and 18 illustrate examples of current source circuits that include compensation circuits but not current sources (although they may be connected to a current source in use, as described in the specification). For example, Fig. 16 illustrates an example of a current source circuit that includes transistor 216_0 and a compensation circuit including transistors 216_1 to 216_3. Similarly, Fig. 18 illustrates an example of a current source circuit that includes transistors 218_1 to 218_n and a compensation circuit including transistors 212_1 to 212_n. Notably, these illustrated circuits themselves do not include the input transistors or current sources referred to by the Examiner (although they may be used in combination with such elements, in some examples).

As illustrated in the example of Fig. 16, claim 19 recites a current source circuit including a first transistor and a compensation circuit. Similarly, as illustrated in the example of Fig. 18, claim 21 recites a current source circuit including a first transistor group and a compensation circuit. Because these claims describe complete current source circuits, as illustrated in the example circuits of Figs. 16 and 18, the claims are complete and do not omit essential elements. While a current source and/or additional input transistors may be used in combination with current source circuits like those illustrated in Figs. 16 and 18 and described in claims 19 and 21, the specification, drawings, and claims of this application clearly describe and illustrate circuits that do not include these additional elements. Accordingly, claims 19 and 21 are fully enabled by the original specification and drawings, and this rejection should be withdrawn.

IV. Rejection Based On 35 U.S.C. § 112, Second Paragraph

Claims 2, 9-11, 17, 19, 21, and 22 are rejected under 35 U.S.C. § 112, second paragraph, as allegedly indefinite. While Applicant does not concede that the claims were deficient under 35 U.S.C. § 112, second paragraph, in order to expedite prosecution and to facilitate allowance of this application, the claims have been amended to clarify various information contained therein. Applicant respectfully submits that the amended claims fully comply with the requirements of 35 U.S.C. § 112. Withdrawal of this rejection is respectfully requested.

While certain claims, such as claims 17 and 21, have been amended herein to recite specific transistors for purposes of clarity, those skilled in the art will recognize that current mirror circuits and current source circuits according to some examples of the invention may include additional components, including additional transistors. For example, as illustrated in Figs. 7, 8, and 15-18, circuits according to some examples of the invention may include numerous transistors in the various transistor groups. Such circuits still may fall within the scope of the present claims.

V. Rejection Based On 35 U.S.C. § 102(b)

Claims 2, 19, and 22 are rejected under 35 U.S.C. § 102(b) based on Guliani, U.S. Patent No. 5,109,187 (hereinafter "Guliani"). Applicant respectfully traverses this rejection and requests its reconsideration.

Applicant's claims 2 and 22 recite current mirror circuits that include a current source; a first MOS transistor having a gate, a drain coupled to the gate and the current source, and a source coupled to a first power source; a second MOS transistor having a gate coupled to the gate of the first

MOS transistor, a drain, and a source coupled to the first power source, wherein a mirror current flows into the drain of the second MOS transistor; and a compensation circuit coupled to the drain of the first MOS transistor and the drain of the second MOS transistor. In claim 2, the compensation circuit is configured to decrease the mirror current against an increase of absolute value of a drain voltage of the second MOS transistor, and in claim 22 the compensation circuit is configured to increase the mirror current against a decrease of absolute value of a drain voltage of the second MOS transistor. Applicant respectfully submits that Guliani does not teach or suggest these claimed arrangements.

As an initial matter, Applicant respectfully submits that Guliani does not teach or suggest a compensation circuit coupled to the drain of a first MOS transistor and the drain of a second MOS transistor, as recited in claims 2 and 22. Additionally, Applicant respectfully submits that Guliani does not teach or suggest that the compensation circuit is configured to decrease the mirror current against an increase of absolute value of a drain voltage of the second MOS transistor (claim 2) or configured to increase the mirror current against a decrease of absolute value of a drain voltage of the second MOS transistor (claim 22), such that the mirror current and the current flowing into the first MOS transistor are the same.

Rather, Guliani describes:

> the start-up circuit [includes] a W-channel device 12, a P-channel device 14 and a W-channel device 16 [ ] coupled to the current mirror section 30 for maintaining the operating point of the circuit 20 in accordance with the diagram in FIG. 3. … <u>The voltage reference circuits such as 20 in FIG. 2 often have a stable state in which 0 current flows in the circuit even when the power supply voltage is non-zero. The start-up circuit is required to prevent the circuit from remaining in this state.</u> As such, the start-up circuit maintains the operating point of the circuit 20 as [close] as possible to operating point V_1 as illustrated in FIG. 3.

See the Guliani Patent at column 5, lines 34-57 [emphasis supplied].

Referring to Fig. 3 in Guliani, Applicant advises that there are two operating points for the circuit 20 in Fig. 2. One is the origin (0,0), and the other is a cross point of IM7 and IM2 whose x-axis value is V1. To prevent the circuit from remaining in the state at origin (0,0) in Fig. 3, a start-up circuit is added to circuit 20. The start-up circuit, which includes W transistor 12, P transistor 14, and W transistor (NOT a PMOS transistor) 16, behaves as a negative feedback circuit. However, the purpose of adding these transistors to the circuit of Guliani is merely to prevent the circuit from remaining in the (0,0) state. Normally transistors 12, 14, and 16 work at start-up, such as at "power-on" of circuit 20, so that the state of the circuit 20 changes from state (0,0) to state x-axis V1. This work is like a "digital" behavior, changing the circuit from one state to the other one. After that, circuit 20 works properly without the start-up circuit. That is why this circuit is called "starter" or "start-up circuit."

Applicant respectfully submits that nothing in Guliani teaches or suggests that the start-up circuit decreases the mirror current against an increase of absolute value of the drain voltage of the second MOS transistor, or that it increases the mirror current against a decrease of absolute value of the drain voltage of the second MOS transistor, as recited in Applicant's claims 2 and 22, respectively. Rather, Applicant submits that Guliani merely discloses changing the state of circuit 20 from state (0,0) to x-axis V1. The W transistor 16 allows current flow, but the current from W transistor 16 is not controlled by a compensation circuit in the manner described in Applicant's claims 2 and 22.

Applicant's claim 19 recites a current source circuit that includes a first PMOS transistor having a source coupled to a first power source, a gate, and a drain coupled to a node; and a compensation circuit. The claimed compensation circuit includes more than one compensation PMOS transistor, wherein each compensation PMOS transistor has a gate, a source coupled to the first power source, and a drain coupled to the node. The compensation circuit further includes more than one subtracter, wherein each subtracter is coupled to the gate of a corresponding compensation PMOS transistor, and each subtracter is configured to supply voltage expressed by an arithmetic series a_k to the gate of the corresponding compensation PMOS transistor, where a_k is the arithmetic series equal to:

$$V_{g1} - kV_{d1} \quad (k = 1, 2, \ldots, n), \text{ wherein}$$

V_{d1} is the drain-source voltage of the first transistor,

V_{g1} is the gate-source voltage of the first transistor, and

n is the number of the PMOS transistors of the compensation circuit.

Applicant respectfully submits that nothing in Guliani teaches or suggests a current source circuit including a compensation circuit as recited in claim 19.

In view of all of the foregoing, Applicant respectfully submits that claims 2, 19, and 22 stand in condition for immediate allowance. Withdrawal of this rejection and allowance of these claims are respectfully requested.

VI. Conclusion

Applicant respectfully submits that this Amendment and the above remarks overcome all of the outstanding objections and rejections in this case, thereby placing the application in condition for immediate allowance. Allowance of this application is earnestly solicited.

If any fees are necessary to facilitate entry and consideration of this Amendment, such as fees under 37 C.F.R. §§ 1.16 or 1.17, the fees can be charged to Deposit Account No. 19-0733. If an extension of time is needed that is not accounted for in the papers filed with this Amendment, then the extension is hereby requested. The necessary extension fee also can be charged to Deposit Account No. 19-0733.

Respectfully Submitted,

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MARKED-UP COPY OF CLAIMS ILLUSTRATING CLAIM AMENDMENTS

Please amend claims 2, 9, 17, 19, 21, and 22 as shown below:

2. (Twice Amended) A current mirror circuit comprising:

a current source;

a first MOS transistor having a gate, a drain coupled to the gate and the current source, and a source coupled to a first power source;

a second MOS transistor having a gate coupled to the gate of the first MOS transistor, a drain, [coupled to a second power source,] and a source coupled to the first power source, the second MOS transistor being the same channel type as the first MOS transistor, a mirror current flowing into the drain of the second MOS transistor, the mirror current corresponding to the current source; and

a compensation circuit coupled to the drain of the first MOS transistor and the drain of the second MOS transistor, the compensation circuit configured to decrease the mirror current against an increase of absolute value of a drain voltage of the second MOS transistor such that the mirror current and a current flowing into the first MOS transistor are the same.

9. (Twice Amended) A current mirror circuit comprising:

a current source;

a first PMOS transistor having a gate, a drain coupled to the gate and the current source, and a source coupled to a first power source, the gate of the first PMOS transistor applied a voltage V_{g1};

a second PMOS transistor having a gate coupled to the gate of the first PMOS transistor, a drain coupled to a [second power source] node, and a source coupled to the first power source, a

mirror current flowing into the drain of the second PMOS transistor, the mirror current corresponding to the current source; and

a compensation circuit comprising:

at least one compensation PMOS transistor, each compensation PMOS transistor having a gate, a source coupled to the first power source, and a drain coupled to the [drain of the second PMOS transistor] node; and

at least one subtracter coupled to the drain of the first PMOS transistor and the second PMOS transistor, each subtracter configured to supply a voltage which is higher than the voltage V_{g1} to the gate-source of each compensation PMOS transistor.

17. (Twice Amended) A current mirror circuit comprising:

a current source;

a first group of [at least two] PMOS transistors connected in series, [wherein each of] the first group of PMOS transistors [has] including:

a first PMOS transistor having a gate, a drain coupled to the gate, and a source, wherein the source of [a] the first PMOS transistor [of the first group of PMOS transistors] is coupled to a first power source, wherein the first PMOS transistor [of the first group of PMOS transistors] is defined as being electrically closest to the first power source in the first group of PMOS transistors, and

a second PMOS transistor having a gate, a drain coupled to the gate, and a source, wherein the drain of the second PMOS transistor is coupled to the current source, wherein

the second PMOS transistor is defined as being electrically closest to the current source in the first group of PMOS transistors;

a second group of PMOS transistors connected in series, wherein the number of PMOS transistors in the second group of PMOS transistors is equal to the number of PMOS transistors in the first group of PMOS transistors, the second group of PMOS transistors including: [each]

a third PMOS transistor [of the second group] having a gate coupled to the gate of [a corresponding] the first PMOS transistor [of the first group], a drain, and a source, wherein the source of [a first] the third PMOS transistor [of the second group of PMOS transistors] is coupled to the first power source, wherein the [first] third PMOS transistor [of the second group of PMOS transistors] is defined as being electrically closest to the first power source in the second group of PMOS transistors, and

a fourth PMOS transistor having a gate coupled to the gate of the second PMOS transistor, a source, and a drain, [wherein the drain of a last PMOS transistor of the second group of PMOS transistors is coupled to a second power source,] wherein the [last] fourth PMOS transistor [of the second group of PMOS transistors] is defined as being electrically furthest from the first power source in the second group of PMOS transistors; [and]

a compensation circuit comprising [:] a third group of PMOS transistors connected in series, wherein the number of PMOS transistors in the third group of PMOS transistors is equal to the number of PMOS transistors in the second group of PMOS transistors, [each of] the third group of PMOS transistors including:

a fifth PMOS transistor having a gate, a source, and a drain, wherein the source of [a first] the fifth PMOS transistor [of the third group of PMOS transistors] is coupled to the first power source, wherein the [first] fifth PMOS transistor [of the third group of PMOS transistors] is defined as being electrically closest to the first power source in the third group of PMOS transistors, and

a sixth PMOS transistor having a gate, a source, and a drain, wherein the drain of [a last] the sixth PMOS transistor [of the third group of PMOS transistors] is coupled to the [second power source] drain of the fourth PMOS transistor, wherein the [last] sixth PMOS transistor [of the third group of PMOS transistors] is defined as being electrically furthest from the first power source in the third group of PMOS transistors; and

a group of subtracters, including:

a first [each] subtracter coupled to the drain of [a corresponding] the first PMOS transistor [of the first group], the source of [a corresponding] the third PMOS transistor [of the second group], and the gate of [a corresponding] the fifth PMOS transistor [of the third group], [each] the first subtracter configured to supply a difference [voltages] voltage between a gate-source [voltages] voltage and a drain-source [voltages] voltage of the [corresponding second group of] third PMOS [transistors] transistor to the gate of the [third] fifth PMOS [transistors in the same position in series as the second group of PMOS transistors respectively] transistor, and

a second subtractor coupled to the drain of the second PMOS transistor, the source of the fourth PMOS transistor and the gate of the sixth PMOS transistor, the second subtractor

configured to supply a difference voltage between a gate-source voltage and a drain-source voltage of the fourth PMOS transistor to the gate of the sixth PMOS transistor.

19. (Twice Amended) A [power] current source circuit comprising:

a first PMOS transistor having a source coupled to a first power source, a gate, and a drain coupled to a [second power source] node; and

a compensation circuit comprising:

more than one compensation PMOS transistor, each compensation PMOS transistor having a gate, a source coupled to the first power source, and a drain coupled to the [second power source and the drain of the first PMOS transistor] node; and

more than one subtracter, each subtracter coupled to the gate of a corresponding compensation PMOS transistor, each subtracter configured to supply voltage expressed by an arithmetic series a_k to the gate of the corresponding compensation PMOS transistor, where a_k is the arithmetic series equal to:

$V_{g1} - kV_{d1}$ $(k = 1, 2, \ldots, n)$, wherein

V_{d1} is the drain-source voltage of the first transistor,

V_{g1} is the gate-source voltage of the first transistor, and

n is the number of the PMOS transistors of the compensation circuit.

21. (Twice Amended) A [power] current source circuit comprising:

a first PMOS transistor group having at least two PMOS transistors connected in series, [wherein] the first PMOS transistor group including:

a first PMOS transistor having a source [of a first PMOS transistor of the first PMOS transistor group is] coupled to a first power source, a gate, and a drain, wherein the first PMOS transistor is defined as being electrically closest to the first power source in the first PMOS transistor group, and

a second PMOS transistor having a source, a gate, and a drain, wherein [a] the drain of [a last] the second PMOS transistor [of the first PMOS transistor group] is coupled to a [second power source] node, wherein the [last] second PMOS transistor is defined as being electrically furthest from the first power source in the first PMOS transistor group; and

a compensation circuit [comprising:] comprising a second PMOS transistor group and a group of subtracters, the second PMOS transistor group having at least two PMOS transistors connected in series, the second PMOS transistor group including:

a third PMOS transistor having a gate, a source, and a drain, wherein [a] the source of [a first] the third PMOS transistor [of the second PMOS transistor group] is coupled to the first power source, wherein the [first] third PMOS transistor is defined as being electrically closest to the first power source in the second PMOS transistor group, and

a fourth PMOS transistor having a gate, a source, and a drain, wherein [a] the drain of the [last] fourth PMOS transistor [of the second PMOS transistor group] is coupled to the [second power source] node, wherein the [last] fourth PMOS transistor is defined as being electrically furthest from the first power source in the second transistor group; and

[a] the group of [subtracters, each subtracter] subtracters including:

a first subtracter coupled to [a] the gate of [a corresponding] the third PMOS transistor, the first [of the second PMOS transistor group, each] subtracter configured to supply a difference [voltages] voltage between a gate-source [voltages] voltage and a drain-source [voltages] voltage of the [corresponding] first [group of] PMOS [transistors] transistor to the gate-source of the [second] third PMOS transistor [which is in the same position in series as the first group of PMOS transistors], and

a second subtracter coupled to the gate of the fourth PMOS transistor, the second subtracter configured to supply a difference voltage between a gate-source voltage and a drain-source voltage of the second PMOS transistor to the gate-source of the fourth PMOS transistor.

22. (Amended) A current mirror circuit comprising:

a current source;

a first MOS transistor having a gate, a drain coupled to the gate and the current source, and a source coupled to a first power source;

a second MOS transistor having a gate coupled to the gate of the first MOS transistor, a drain [coupled to a second power source], and a source coupled to the first power source, the second MOS transistor having the same channel type as the first MOS transistor, a mirror current flowing into the drain of the second MOS transistor, the mirror current corresponding to the current source; and

a compensation circuit coupled to the drain of the first MOS transistor and the second MOS transistor, the compensation circuit configured to increase the mirror current against a decrease of

absolute value of a drain voltage of the second MOS transistor <u>such that the mirror current and a current flowing into the first MOS transistor are the same</u>.